# Research and Development Section
# Indian Institute of Technology Guwahati
# Guwahati-781039, Assam

Applications are invited for a **Walk in interview** for the following post(s) in the project entitled, **"Performance and energy optimization in many core processors using dynamic cooperation of cache memory, NoC and DRAM controller"** at the department of Computer Science and Engineering, IIT Guwahati.

**Date: 24 May 2019 (Friday)**
**Time: 1 pm**
**Venue: CSE Department**

| Sl. No. | Project Staff Designation | Number of Vacancies | Pay Recommended (Rs.) | HRA Required (Rs.) | Medical Required (Rs.) | Total Amount (Rs.) | Duration of Appointment in months | Qualifications |
|---|---|---|---|---|---|---|---|---|
| 1 | JRF (GATE) | 1 | 31000 | Yes Rs. 4960 | 1250 | 37210.00 | 6 | Candidate should have one of the following qualifications. 1. B.Tech in CSE/ECE/IT with a valid GATE score or 2 year of work experience. 2. M.Tech in CSE/ECE/IT |

**How to apply and selection process:** Candidates have to appear in the Walk in Interview along with an application/CV on plain paper giving details of all educational qualifications, experience, contact address, phone no., E - mail etc. and submit photocopies of relevant documents at the time of interview on 24 May 2019 (Friday) at 1 pm. Venue: CSE Department . Selection will be based on the performance of the candidate in the interview. Candidates will not be sent any call letter separately. Advance copy of CV may be sent to the Principal Investigator.

For any clarification, contact: John Jose (Principal Investigator)
Email: johnjose@iitg.ac.in
Phone: 9048665842

**No campus accommodation will be available for the selected candidates.No TA/DA will be paid to the candidates for appearing in the test and interview.**

**xCSESPNSERB01125xxJJ002** **Asstt. Registrar(R&D)**